The internal bus bridge enable flip-flop 106 provides an internal bus bridge enable signal 162 to the internal I/O circuit 140 that allows the bus bridge 120 to issue a second internal signal via a second internal signal path (a first portion of the bufferless data path 122) and an output buffer 164 over the AGP bus extension 192. The internal bus bridge data-out flip-flop 102 aligns the data to comply with the AGP bus protocol, if necessary, within the bus bridge 120 pending issue of the data over the AGP bus 190 (shown in FIG. 4). The signal at the data input of the output buffer 164 is shown connected to the data input of the internal circuit data in flip flop 110, and is driven from the internal bus bridge data out flip flop 102. Any arrangement that affords the bus bridge 120 being able to send a signal to the input of the output buffer 164, and a logically similar signal to the input of the internal circuit data in flip flop 110, applies.

IN THE CLAIMS:

Please amend Claim 2, Claim 21 and add new Claim 40 to read as follows:

2. (Amended) The configurable interface circuit of Claim 1, further comprising:

an output buffer operative to receive the first internal signal via a second internal signal path and to provide the second internal signal via the first external signal path.

21. (Amended) A method for configuring a bus interface circuit comprising:

at an internal circuit, receiving a bus bridge signal from an internal bus bridge; and

at an internal I/O circuit, preventing signals from any external circuit from reaching the internal circuit.

40. (New) A configurable interface circuit comprising:

an internal graphics controller operable to provide a first internal signal via a first internal signal path;

an input buffer operable to receive a first external signal via an first external signal path;

a selector circuit coupled to the internal graphics controller via the first internal signal path, and to the input buffer, the selector circuit operable to select either the first internal signal or the first external signal to provide a selected signal;